CHRP I/O Device Specification Version 1.0
Change Notice

October 2, 1996

Apple/IBM/Motorola - CHRP Board

This paper presents a chronological list of all changes approved for the published version of the *PowerPC Microprocessor Common Hardware Reference Platform: I/O Device Reference* (I/O Device Specification). These changes are approved by the CHRP Board. These changes will be incorporated into the next version of the document at the next printing of the CHRP specification.

SCC Corrections

This Architecture Change Request (ACR00008) was approved by the CHRP Board on June 6, 1996.

Issue

Changes are required to document actual Apple SCC registers and their offsets and to clarify the relation between the SCC and the 85C30 chip.

Changes

- Change “ESCC” to “Apple SCC” throughout:
  - p. 115, Chapter title and lines 1, 2, 5, 7, 8, 10, 12, 16, and 22
  - p. 116, Section 9.2 head and lines 1, 4, 5, and 8
  - p. 117, Section 9.3 head and Table 222 caption
  - p. 118, Section 9.4 head, Table 223 caption, and Table 224 caption
  - p. 119, Section 9.5 and 9.7 heads, Table 225 caption, and line 10
  - p. 120, lines 1 and 2
  - p. 121, Section 9.8 head and lines 1, 5 (twice), 7, 8, and 9
  - p. 124, Table 241, column 2, lines 3 and 5
  - p. 125, Table 243 (continuation), column 2, lines 3 and 5
  - p. 125, Table 245 , column 2, lines 3 and 5
  - p. 126, Line 1
  - p. 126, Table 249, column 2, lines 1, 3, 5. 7, 9, 11, 13, and 15
  - p. 127, Section 9.9 head and line 1
  - p. 128, Numbered items 2, 4, 6, 8, 9, and 14
  - p. xxv, bullet for Chapter 9
  - p. 147, third line from bottom of page
- On page 115, lines 2-3: Change “an enhanced” to “a modified”.
- On page 117: Table 222 should read as follows:

Table 222. Apple SCC Registers

Offset	Register	Open Firmware Reg Property
0x000	Command B	
0x010	Data B	
0x020	Command A	
0x030	Data A	
0x040	Channel B Enhancement	
0x050	Channel A Enhancement	
0x080	SCC Recovery Count	
0x090	LTPC Start A	
0x0A0	LTPC Start B	
0x0B0	LTPC Detect AB	
0x100	Timer A	
0x110	Timer B	reg[1],size=4096
0x120	Special Character 1A	
0x130	Special Character 2A	
0x140	Special Character 3A	
0x160	Special Detect A	
0x180	Special Character 1B	
0x190	Special Character 2B	
0x1A0	Special Character 3B	
0x1C0	Special Detect B	
0x1D0	Receive Mask A	
0x1E0	Receive Mask B	
See Section 15.4.1, “Register Organization,” on page 173	Channel A DBDMA Tx Registers	reg[2],size=256
	Channel A DBDMA Rx Registers	reg[3],size=256
	Channel B DBDMA Tx Registers	reg[4],size=256
	Channel B DBDMA Rx Registers	reg[5],size=256

- On p. 118: Table 223 should read as follows:

Table 223. Apple SCC Legacy Registers

Offset	Register	Open Firmware Reg Property
0x000	Command B	
0x002	Data B	
0x004	Command A	
0x006	Data A	
0x008	Channel B Enhancement	
0x00A	Channel A Enhancement	
0x080	SCC Recovery Count	
0x090	LTPC Start A	
0x0A0	LTPC Start B	

Table 223. Apple SCC Legacy Registers ***(Continued)***

Offset	Register	Open Firmware Reg Property
0x0B0	LTPC Detect AB	
0x100	Timer A	
0x110	Timer B	reg[1],size=4096
0x120	Special Character 1A	
0x130	Special Character 2A	
0x140	Special Character 3A	
0x160	Special Detect A	
0x180	Special Character 1B	
0x190	Special Character 2B	
0x1A0	Special Character 3B	
0x1C0	Special Detect B	
0x1D0	Receive Mask A	
0x1E0	Receive Mask B	
See Section 15.4.1, "Register Organization," on page 173	Channel A DBDMA Tx Registers	reg[2],size=256
	Channel A DBDMA Rx Registers	reg[3],size=256
	Channel B DBDMA Tx Registers	reg[4],size=256
	Channel B DBDMA Rx Registers	reg[5],size=256

- On p. 119, Table 224: last block in column 1 should read: "See Sec 15.4.1 on page 173"
- On p. 120, Section 9.7.1 heading change to "Command A and B Registers"
  - On p. 120, change sentence after Table 226 to "The Command registers are used to pass byte wide commands to and from devices on the SCC channels."
- On p. 120, Section 9.7.2 heading change to "Data A and B Registers
  - p. 120, change sentence after Table 227 to "The Data registers are used by the DMA engine and by system software to send and receive bytes to the SCC port."
- On p. 120, Section 9.7.3 heading change to "Enhancement A and B Registers"
  - p. 120, change sentence after table 228 to "These registers are needed for GeoPort and are described in Table 229."
- On p. 121, Table 230: Change Offset Address from "0x60" to "0x080".
- On p. 122, Table 232: Change Offset Address from "0x70" to "0x090".
- On p. 122, Table 234: Change Offset Address from "0x80" to "0x0A0".
- On p. 123, Table 236: Change Offset Address from "0x90" to "0x0B0".
- On p. 123, Section 9.8.5 head: Change to "Timer A and B Registers".
  - p. 123, Table 238: Change Offset Address to "0x100, 0x110"
  - p. 123, After Table 238: change the sentence to reference the right table as follows "Table 239 on page 123 gives the format of these registers."

— p. 123, Table 239: Change caption to “Timer Registers”.

- On p. 124, Section 9.8.6 head: Change to “Special Character 1A and 1B Registers”.
  - — p. 124, Table 240: Change Offset Address to “0x120, 0x180”.
  - — p. 124, After Table 240: Change line “Table 241... these registers”.
  - — p. 124, Table 241: Change caption to “Special Character 1 Registers”.
- On p. 124, Section 9.8.7 head: Change to “Special Character 2A and 2B Registers”.
  - — p. 124, Table 242: Change Offset Address to “0x130, 0x190”.
  - — p. 124, After Table 242: Change line “Table 243...these registers”.
  - — p. 124, Table 243: Change caption to “Special Character 2 Registers”.
- On p. 125, Section 9.8.8 head: Change to “Special Character 3A and 3B Registers”.
  - — p. 125, Table 244: Change Offset Address to “0x140, 0x1A0”.
  - — p. 125, After Table 244: Change line “Table 245...these registers”.
  - — p. 125, Table 245: Change caption to “Special Character 3 Registers”.
- On p. 125, Section 9.8.9 head: Change to “Special Detect A and B Registers”.
  - — p. 125, Table 246: Change Offset Address to “0x160, 0x1C0”.
  - — p. 125, last line: Change to “When bits 0, 1 or 2 are set as described in Table 247 on page 126 an interrupt to the system is generated”.
  - — p. 126, Table 247: Change caption to “Special Detect Registers”.
- On p. 126, Section 9.8.10 head: Change to “Receive Mask A and B Registers”.
  - — p. 126, Table 248: Change Offset Address to “0x1D0, 0x1E0”.
  - — p. 126, Table 249: Change caption to “Receive Mask Registers”.
- On p. 127: Table 250 should read as follows:

Table 250. Apple SCC DBDMA Transmit Channel Status Bits

Bit	Meaning
s7	1= the timer has decremented to 0; 0=the timer is still decrementing
s6	1=GPIOA is low into the serial port; 0=GPIOA is high
s5	the LTPC has detected the end of a LocalTalk packet
s4 ... s1	not implemented
s0	Wait (externally controlled)

- On p. 255, delete the line “ESSC Extended ...”
- On page 257, reword the SCC definition to “Apple serial communication controller”

Note: Because this change is extensive, the CHRP board agreed to include it in a update to the *PowerPC Microprocessor Common Hardware Reference Platform: I/O Device Reference* document. This change will be incorporated in the electronic version during July 1996. This modification will be called Version 1.01.

Delete the special 87308 software implementation note

This Documentation Error Report (DER00001) was approved July 8, 1996.

Issue

A Software Implementation Note and compatible property were documented to take care of the case that a National 87308 was used. Analysis of the chip logic indicated they are no longer needed.

Changes

- On page 80, delete the last sentence of requirement 5-1 which reads “The compatible property may also specify the compatible property for the National Semiconductor 87308 in addition to ‘chrp,ecp’”
- On page 89, delete the Software Implementation Note about the 87308 (includes the 5 numbered items).

UART serial device interrupt definition.

DER00003 was approved by the CHRP Board on July 17, 1996.

Issue

Requirement 6-3 requires the UART serial device to generate a low-to-high edge-sensitive interrupt. The legacy UART (16550) actually generates a high-active level interrupt.

Historically, all ISA interrupts were treated as +edge sensitive even though some were +level at the source (this still works). The intent of Requirement 6-3 was to propagate that model, but it didn’t come out correctly.

Change

- Reword requirement 6-3 as follows:

6-3. The UART serial device must generate an interrupt that is compatible with a low-to-high edge sensitive interrupt request input at the interrupt controller.

Detect AB Corrections

ACR00010 was approved by the CHRP Board on July 26, 1996.

Issue

Changes are required to resolve ambiguities and inaccuracies in the existing SCC chapter.

Change

- On page 123, Table 236 in “Read/Write Characteristics” column, change “Read/Write” to “Read Only”.
- On page 123, Section 9.8.4 change the text to the following:

“The 2-bit read-only register shown in Table 237 consists of separate Detect A and Detect B bits. They indicate whether the LTPC has detected the abort sequences for the corresponding transmit channels. Both bits are cleared on reset and each bit is set when the LTPC logic has been armed (by setting the Start register) and has then detected the abort sequence. Each bit stays set until the corresponding Start register is cleared by software.”

- On page 116, Requirement 9-2 the value “3.684” should be “3.6864”.

Corrections to ISA Keyboard Mouse

ACR00026 was approved by the CHRP Board on September 23, 1996.

Issue

Various typographical errors exist in Chapter 7 which make it appear that the 8042 is not being supported.

Change

- In the chapter replace all instances of “output buffer” with “output register”
- Section 7.3.2 - Change the table reference in the paragraph to table 213. The paragraph should now read “Table 213 on page 108 defines ... Input Register.” Note that this error is due to a Frame Maker bug and the title and cross reference must be erased and reentered to correct this line.
- Section 7.3.3 - Change the table reference in the first paragraph to Table 215. “Table 215....Status Register.” Same bug.
- Change the title of table 215 to “Controller Status Register” because this term is used other places.
- Rewrite the description of bit 7 and 6 to be consistent with the Surepath description:
- In table 215 for bit 4 the meaning of 0 and 1 was reversed and the phrase “Keyboard Lock Status” is redundant and should be removed.
- Bit 2 should have the phrase “System Flag (SYSF): bold and should reference table 218+1.
- Bit 1 should say “IN register”. The corrected table is below.

Table 215. Controller Status Register (STA)

Bit	Normal Function	Special Function
7	**Parity Error:** When set to 0, this bit indicates that the last byte of data received from the device had odd parity. When a parity error occurs, this bit is set to 1.	See the Self-Test command in Table 218 on page 109 for a description of these bits if an error is detected on self-test.
6	**General Time-out:** When set to 1, this bit indicates that a transmission was started by the device, but did not finish within the received time-out delay or was started by the controller, but the byte transmitted was not clocked out within the specified time limit. The controller indicates a time-out if: • The byte was clocked out, but a response was not received within the time limit. • The byte was clocked out, but a response indicates a parity error (bit 7 is also set)	
5	**Auxiliary Byte (AUXB):** When this bit is a 1 and OUTB is a 1, the OUT register contains data from the auxiliary device (mouse). When it is a 0 and OUTB is a 1, it contains keyboard data or command controller response data from the 8042.	
4	**Keyboard Lock (KEYL):** When this bit is a 0, the keyboard is locked and the password state is active. When this bit is a 1, the keyboard is free.	
3	**Command/Data (C/D):** When this bit is a 1, it indicates a command has or will be written to the IN register. When this bit is a 0, it indicates that data has or will been written to the IN register C/D (Command/Data)	N/A
2	**System Flag (SYSF):** This bit is set to a 1 or 0 by writing to the system flag bit (bit 2) in the Controller Command byte. Refer to Table 218+1.	N/A
1	**Input Byte (INPB):** When this bit is a 1, the system has put data in the IN register for the keyboard	N/A
0	**Output Byte (OUTB):** When this bit is a 1, the keyboard/mouse has put data in the OUT register. If this bit is a 0, the OUT register is empty (the system has read the last byte presented in the OUT register).	N/A

- Section 7.3.4 Replace the sentence and Table 217 with “The commands defined in Table 218 are written to this register.
- Table 218 Codes 0x20 and 0x60 need to reference a new table (218+1). Remove the parenthesis around the sentence in 0x60 and reword.
- Code A7 and A8 should use the phrase “Controller Command Byte”
- Code AA has two periods at the end of the first sentence.
- Code C0 in Table 218 should reference a new table 218+2.
- Code D0 should reference Table 219 and should be reworded. “”
- Code 0xD1 should be reworded and refer to table 219.
- Code 0xD2 should be reworded.
- Code 0xD3 should be reworded.
- Remove the second sentence, “An interrupt occurs..”, in the description of 0xD4.
- Code E0 spelling “represents”
- An updated table 218 is included below.

Table 216. Controller Commands

Code	Command	Description
0x20-0x3F	Read Controller RAM	Bits 5-0 of this command specify the address that the controller will use to address data returned in the output register. Internal address 0b00000 is assigned as the Controller Command Byte, refer to Table 218+1.
0x60-0x7F	Write to Controller RAM	Write to Controller|Bits 5-0 of this command specify the internal address to which the controller will write. The next byte of data placed in the input register will be written to this address. Internal address 0b00000is assigned as the Controller Command Byte, refer to Table 218+1.
0xA4	Reserved	
0xA5	Reserved	
0xA6	Reserved	
0xA7	Disable Auxiliary Device (Mouse)	This command sets bit 5 of the Controller Command Byte to 1. This disables the auxiliary device interface by driving the clock line low. Data is not received while the interface is disabled.
0xA8	Enable Auxiliary Device (Mouse)	This command sets bit 5 of the Controller Command Byte to 0, releasing the auxiliary device interface.
0xA9	Check Interface to Auxiliary Device (Mouse)	Checks the interface to the auxiliary device and stores the check code in the output Register: 0x00=no error 0x01=clock line stuck low 0x02=clock line stuck high 0x03=data line stuck low 0x04=data line stuck high
0xAA	Self-Test	The keyboard controller executes a self-test and writes 0x55 into the output Register if no error is detected. Bit 0 of the Controller Status Register is set to a 1 upon completion of the self-test. The system should allow one second for the self-test to complete before assuming an error occurred and checking the Controller Status Register bits 7-4 for t he error indication. Bits 7-4 of Controller Status Register if error occurs: 0x1 - Valid 0xAA self-test command check 0x2 - Controller instruciton processing tests 0x3 - RAM data and addressing tests 0x4 - ROM data checksum and addressing tests 0x5 - Timer and interrupt handling tests 0x6 - Initialization routines and checks 0x8 - Self-test complete and 0x55 placed in the output register
0xAB	Check Keyboard Interface	Checks the interface to the keyboard device and stores the check code in the output Register: 0x00=no error 0x01=clock line stuck low 0x02=clock line stuck high 0x03=data line stuck low 0x04=data line stuck high
0xAD	Disable keyboard	Disables the keyboard. and sets bit 4 of the Controller Command byte to 1.
0xAE	Enable Keyboard	Enables the keyboard. and sets bit 4 of the Controller Command byte to a 0.
0xC0	Read Input Port	Reads the input port to the keyboard/mouse and transfers the data into the output Register. Refer to Table 218+2.
0xC2	Poll Input Port (high)	Reads bits 7-4 of the input port from the device and transfers them into bits 7-4 of the status register.
0xC3	Poll Input Port (low)	Reads bits 3-0 of the input port from the device and transfers them into bits 7-4 of the status register.
0xD0	Read Output Port	Reads the output port and places the data in the output register. Refer to Table 219.
0xD1	Write Output Port	Writes the following data byte in to the ouput port.

Table 216. Controller Commands ***(Continued)***

Code	Command	Description
0xD2	Write Keyboard Output Register	The next byte of data written to the input regiister is written to the output register, as if initiated by the keyboard (clears AUXB in the status register). An interrupt occurs if keyboard interrupts are enabled in the Controller Command Byte.
0xD3	Write Ouput Register to Auxiliary Device (Mouse)	The next byte of data written to input register is written to the output register, as if initiated by the auxiliary device(AUXB in the status register is set). An interrupt occurs if auxiliary interrupts are enabled in the Controller Command Byte.
0xD4	Write Auxiliary Device	Writes the following byte into the auxiliary device.
0xE0	Read Test Input Port	This command causes the keyboard/mouse controller to read its test inputs and place the results in the output register. Test 0 (T0) is connected to the keyboard clock line, and test 1 (T1) is connected to the auxiliary device clock line. Data bit 0 represents T0, and data bit 1 represents T1.
0xF0-0xFF	Send Pulses to Output Port	This command pulses selected bits in the keyboard/mouse controller ouput port (to the device) for approximately 6 microseconds. Bits 3-0 of this command select the respective bits in the output port .

- Add Table 218+1 which defines the byte for these commands

Table 218+1. Controller Command Byte

Bit	Description
7	Reserved
6	Keyboard Translate: When this bit is set to 1 the controller should translate the incoming scan from set 2 to set 1.
5	Disable Auxiliary Device: When this bit is set to 1, the |auxiliary device is disabled.
4	Disable Keyboard: When this bit is 1, the keyboard is disabled.
3	Reserved
2	System Flag: The value written to this bit is placed in the system flag bit of the Controller Status register.
1	Enable Auxiliary Interrupt: When this bit is set to 1, the controller generates an interrupt when it places auxiliary device data in its output register.
0	Enable Keyboard Interrupt: When this bit is set to 1, the controller generates an interrupt when it places keyboard data in its output register.

- Add Table 218+2 whcih defines the input port

Table 218+2. Input Port

Bits	Description
7-2	User Definable
1	Auxiliary Data In: Reflects the state of the auxiliary data line
0	Keyboard Data In: Reflects the state of the keyboard driven data line

- Change the title of Table 219 to “Output Port”.

- In Table 219 add colons and remove parenthesis on bits 5 and 4 for consistency.
- In Table 219 remove double colons on Bit 3 and 2.
- In table 219 change the description for bit 1and 0.
- Table 219 as updated is included below.

Table 219. Output Port

Bit	Description
7	Keyboard Data Out : Reflects state of this data line to the keyboard.
6	Keyboard Clock Out : Reflects state of this clock line to the keyboard.
5	Auxiliary Device Interrupt: When this is 1 an interrupt has been generated by the auxiliary device in the output register.
4	Keyboard Interrupt : When this is 1 an interrupt has been generated by the keyboard device putting data in the output register or any connected device posting a command to the output register.
3	Auxiliary Clock Out: Reflects state of this data line to the auxiliary device.
2	Auxiliary Data Out: Reflects state of this clock line to the auxiliary device.
1	Gate Address Line A20: No function in CHRP systems.
0	Reset System: No function in CHRP systems.

This is the last page of the CHRP I/O Device Specification Version 1.0 Change Notice