PowerPC Reference Platform Specification
Version 1.1

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Preface

This version of the *PowerPC Reference Platform Specification* includes changes and enhancements which have been suggested by reviewers within the team which is developing this specification. In addition, valuable suggestions and experience have been obtained by interacting with users of this specification and from participants in classes on this subject. This information has been incorporated into this version of the specification.

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Summary of Changes

Table 1 lists changes for each version of this document from the initial Alpha Release in November 1993. Changes which are clerical are not listed. Within the text, changes which have been made for the current Version 1.1 are marked with a "|" symbol. Changes which were made for Version 1.0 are marked with a "/" symbol.

Table 1 (Page 1 of 9). History of Changes to the Specification

Content of the Change	Reason for the Change
Changes for the Beta Version of the specification	
Added Workplace OS material to the appendix and summarized it in the System Configuration section.	This material was not available for the Alpha release.
Changed processor designation to "PowerPC 601."	This is a vendor-neutral designation.
Changed heading and initial paragraph for Section 3.17, "PowerPC Architecture Features Not Recommended."	To clarify that these were system recommendations and not processor recommendations.
Redrew portable diagram to match implementations.	To create a family resemblance in implementations.
Added AIX memory map restrictions to the appendix and the memory map architecture section.	AIX requires reserved memory.
Changed the hardware configuration section -- used the term "alphanumeric device" instead of keyboard.	This is an implementation-independent term.
Showed recommendation for parity and ECC memory.	This subject was not addressed.
Changed "main memory" to "system memory" in the multiprocessor appendix.	To make consist with the definitions in the memory map section.
Made modifications of the I/O Master view of the Memory Map figure.	There was an error in the location of Flash ROM.
Changed title of Section 2.9, "Industry Interface Standards," and defined keyboard interfaces as examples.	List of keyboard interfaces was not complete.
Identified specific IDE standard.	To provide definition of IDE standard.
LocalTalk added to Table 4 as recommended.	LocalTalk needed on other configurations.
Added Ethernet adaptor and removed "ISA."	Section on Compliant Subsystem and Devices does not show IBM 16-bit and Ethernet adaptors.
Serial ports 3 and 4 added to Table 14	Serial ports 3 and 4 were not covered in Reference Implementation.
Modified the Workstation and Portable reference implementations.	To explain the number of sync instructions in the PowerPC 601 Endian switch example and to show an example for other processors.

Table 1 (Page 2 of 9). History of Changes to the Specification	
Content of the Change	**Reason for the Change**
Section deleted.	Firmware development information is not architecture and is too product-specific.
Spelled out MCA on first use and put in acronym table.	To differentiate from Music Corporation of America.
Added statement to require an abstraction.	To clarify that the software must protect self modified code from loss of coherency.
Referenced the different PCI buses in the figure for the technical workstation description in the appendix.	The description for a technical workstation's reference implementation needs to clarify that there are two PCI buses.
Some clarification added.	Some of the features in the section on Power Management Hardware Features needed to be clarified.
Clarified the effect on hardware and software if the operating system does not have an abstraction layer accessible to third parties.	Clarified the second note in the System Abstraction Layer section.
Clarified that direct store segments support is an option.	Previously unclear whether direct store support was required.
Clarified that cache inhibited string operations to System Memory do not need to be supported.	Inconsistency in the description of handling string operations.
Wording changes and references to the PowerPC architecture in the Hardware Configuration section.	Requirements are not clearly defined in the Hardware Configuration section.
Changed "should" to "recommended."	To make terminology consistent in the configuration and architecture sections.
Clarified the alignment requirements.	The alignment requirements reference an implementation and the rationale needs to be defined.
Made changes to Reference Implementation to address what was implemented and eliminated architectural alternatives.	Reference Implementation gave too many architectural alternatives.
Changed figure and description for ISA I/O master access to memory.	Description and figure for I/O masters did not match.
Included an energy-managed workstation in the appendix and deleted some equipment from the portable description.	The portable configuration described in the appendix contained components not found on portables.
Described the Bi-Modal graphics adaptor approach in the Endian appendix.	Need to describe Bi-Modal graphics adaptors.
Improved descriptions of AIX.	AIX appendix did not define the scope and version.
Edited for clarity in the Upgrade Slot Definition.	Some of the L2 cache protocol is not clear.
Inserted the map of the CMOS RAM in the Reference Implementation.	The map of CMOS RAM was not included.
Added new figures and text in the Machine Abstraction section.	To clarify the abstraction software requirements.

Table 1 (Page 3 of 9). History of Changes to the Specification	
Content of the Change	**Reason for the Change**
The tables in the operating system appendices and in the Hardware Configuration section were changed to remove VGA and allow 640-by-480 resolution.	To clarify graphics requirements for operating systems' hardware.
Added stand-alone diagnostics to "Configuration and Diagnostics."	Single user workstations may not need on-line diagnostics.
Audio subsystems in reference platform and portable implementation example now use Crystal Semiconductor CS4231 audio integrated circuit.	Design change.
Added description of Scatter/Gather DMA.	Clarification.
Deleted references to VGA Hardware Emulation.	VGA Hardware Emulation components were deleted from the design.
Clarified upgrade slot information.	Upgrade slot does not support multiprocessing.
Added an implementation example for MP Interrupts.	Additional level of detail.
Rewrote most of the Power Management section in architecture.	Rewrite was due to results of PM review meetings.
Provided details of support for suspend and hibernate states.	Clarification.
VPD section in Firmware section was moved to residual data section.	VPD is defined in residual data structure.
Defined NVRAM structure.	Definition of NVRAM was required.
Re-wrote Architecture Compliance Testing.	Added four phases of testing. Added section on branding.
Tagged index items and created index in the back of the document.	Index needed.
Changed "60x" to "PowerPC" or "PowerPC processor."	"60x" does not take into account 620 or future products.
Changed "CPU bus," "60x bus," "local bus" to "primary processor bus" or "PowerPC processor bus."	"60x" incorrect; consistency needed.
Changed RTC to NVRTC in Section 6.	NVRTC more accurate and not confused with 601 RTC.
Changed "conflict" to "corrupt" and "NT" to "Windows NT" in Section 6.	Clarification.
Changed "memory access" to "system memory address" in Section 6.	To ensure consistency and avoid confusion.
Removed "h" from hex nomenclature and changed "cache line" to "buffer line" in Section 6.	For consistency and clarification.
Deleted rows from System I/O Address Map table pertaining to "VGA Emulation."	Changed to reflect current I/O Address Map.

Table 1 (Page 4 of 9). History of Changes to the Specification	
Content of the Change	**Reason for the Change**
Created acronym table.	To define acronyms for readers unfamiliar with them.
Created glossary.	To define terms and make specification usable to a diverse audience.
Added new information to Multiprocessor section in appendix.	More detail regarding symmetric multiprocessor systems needed.
Portable System section in Appendix A replaced with updated information.	For clarification and additional information.
Title of Section 3 changed to "Architecture Guidance."	"Guidance" clarifies intent of section.
New language inserted in Section 1.1 regarding interfaces.	Illustrates that key features of PowerPC Reference Platform architecture include use of industry standard interfaces.
New language added to Section 3.1 regarding system memory coherency.	Previously omitted.
Language in Appendix C regarding operating systems removed.	Necessary correction.
GTX Graphics Subsystem added to PCI Adapter list in Appendix C.	Previously omitted.
Rearranged information regarding multiprocessor interrupts in Section 3.	This information was extensive enough to warrant its own subsection.
Added information to multiprocessor section regarding in-line L2 caches.	To explain the need for in-line L2 caches in SMP systems.
/ Changes for Version 1.0	
/ Updated Appendix F and Hardware Configuration / sections to clarify the requirements to support / Workplace OS.	Some of the Workplace OS requirements were not clear.
/ Reorganized and reworded the subsystem / description in Section 2.	Requirements were not crisply defined in the Hardware Configuration section.
/ Changed to a software-controlled setting of frame / buffer and graphics registers in Section 2.4.4	Independent setting of the frame buffer and graphics registers is not required.
/ Clarified information regarding hardware / coherency in Section 2.2.4.	I/O memory on the processor bus may not always participate in the hardware coherency.
/ Changed the table of contents to just chapters and / major sections within a chapter.	Table of contents was too detailed.
/ Several wording changes such as "directly / attached" changed to "directly attached or / built-in" in the Hardware Configuration section.	Some wording in the Hardware Configuration section does not consider portables.
/ Added a recommendation to provide scrolling / capability.	Portable display devices may not have resolution as high as the recommended resolution.
/ Described the branding and certification in the / Introduction.	Verification is not architecture.

Table 1 (Page 5 of 9). History of Changes to the Specification	
Content of the Change	**Reason for the Change**
Reformatted chapter 2 and 3 to separate requirements.	Chapter 2 and 3 did not clearly define requirements.
Clarified the time base in the processors.	Time base runs at a slower frequency than the processor bus.
Defined system requirements of I/O access from the processor.	Bus bridge requirements were not clear.
Added warning that some operating systems do not maintain coherency.	AIX expects hardware-maintained coherency.
Increased the minimum hardfile size to 120 MB.	Hardfile size was too small for any operating system.
Clarified hardfile implementation information.	“Hardfile” may imply only spinning media.
Defined hardfile size as formatted, uncompressed space.	Hardfile size was not specific.
Media detection requirement added.	Some operating systems use media detection.
Indicated ISO 9660 required software support.	ISO 9660 does not effect the hardware configuration
Recommended wiring the CD-ROM directly to the audio subsystem.	Reference Implementation designed this way.
Clarified pointing device requirements.	Pointing device requirements were not clear.
Clarified and expanded audio requirements.	Audio requirements were not precise and need more description.
Added Bi-Endian graphics adaptor requirement.	Big-Endian applications which write directly to graphics need Big-Endian adaptors.
Made parallel port optional.	A smaller footprint is possible without a parallel port.
Clarified DMA controller information.	DMA controllers should not alias.
Recommended the enhanced IDE.	Enhanced IDE will have several advantages.
Added and updated references in Section 2.9.8.	PCI and PCMCIA references needed to be updated.
Added PCMCIA information in Section 2.9.9.	The PCMCIA requirements needed to be expanded.
Added Solaris information to Chapter 2 and Appendix G.	Solaris information was missing.
Explained the software impact of storage combining in Section 3.2.	The architecture allows storage combining.
Defined the code sequence for synchronizing the I and D cache in Section 3.5.	It was not clear why an operating system service is needed.
Added information regarding Bi-Endian design in Section 3.12.	The impacts on software of Bi-Endian design were not completely defined.
Defined terms and corrected errors in the tables in Section 3.15 and 3.16.	It was not clear what combinations of size and address the system hardware must support.

Table 1 (Page 6 of 9). History of Changes to the Specification	
Content of the Change	**Reason for the Change**
Included the device drivers in the RTAS definition in Section 4.4.	Device drivers provide an abstraction function.
Abstraction only required in Section 4.4.3, if the operating system manages coherence.	Flushing buffers is not supported by some operating systems.
Provided for alternate sources of PCMCIA Socket Services.	Some operating systems supply PCMCIA Socket Services device drivers.
Added new appendix section.	provide information about the PowerPC Binding to IEEE 1275.
Added discussion of implementation attributes of coherence.	Subtleties of maintaining coherence needed to be explained in Section 3.2.
Noted that the 601 prefetches as if storage was not guarded.	Section 3.3 required clarification that the 601 treats storage as not guarded.
Defined operation in an environment with load and store combining.	Load and store combining has an effect on System I/O, Section 3.4.
Clarified the approach for bus resource locking.	Section 3.6 needed to define bus resource locking.
Section 3.8 -- defined addresses for 64-bit implementations.	A 64-bit address space may change addresses.
Section 3.8 now recommends an approach for abstracting the memory map.	Memory map is not defined in the architecture.
Indicated that software must program to the weakly ordered model.	Section 3.9 indicated that systems must be weakly ordered.
Noted changes in the approach for supporting hibernation and suspend.	Section 3.11.1 was not consistent with the current implementations.
Clarified the software and hardware support for power management.	Section 3.11.3 needed to be clarified.
Defined Bi-Endian requirements and implementation.	Section 3.12 must allow all Bi-Endian implementations.
Restructured Section 3.13.	Section 3.13 has some non-multiprocessor information and implementation information.
Defined the requirements for a bridge in Section 3.15 and added load and store combining considerations.	To define the specific requirements.
Defined the requirements for a bridge in Section 3.16 and corrected some entries in the table.	To define the specific requirements.
Clarified that non-word-aligned floating-point uncached loads or stores need not be supported.	Section 3.17.6 does not allow word-aligned floating-point.
Clarified that the special direct store should be encapsulated.	Section 3.17.8 must allow use of the special direct-store segment.
Added clarification in Section 4.1.	It was not clear that hardware vendors are responsible for supplying replacement abstraction.
Allowed for PCMCIA device drivers.	Section 4.4.12 did not discuss PCMCIA drivers.

Table 1 (Page 7 of 9). History of Changes to the Specification	
Content of the Change	**Reason for the Change**
Reworked Section 5.0 to include the Open Firmware requirement and describe both the conventional (i.e. legacy) approach and Open Firmware approach.	Open Firmware should be made a requirement.
Defined the addressing state in Section 5.4.1.	The addressing mode at the end of boot was not clear.
Added Section 5.4.2, which defines the conditions for getting service from Open Firmware during run-time.	Open Firmware may supply some function during run-time.
Added Section 5.5.5.2 to describe NVRAM.	The NVRAM header file is hard to read.
Section 5.6 notes that Open Firmware will replace Residual data.	Open Firmware supplies information which is also contained in Residual data.
Added section 5.6.2.	Some terminology in Residual data is Plug and Play.
Added section 5.7 to describe Open Firmware.	Open Firmware is in the appendix.
Defined serial port addresses and reserved some addresses.	Section 6.1.5 does not define all serial port addresses.
Made changes in Sections 6.1.5.3, 6.1.5.8, and 6.1.5.9.	The meaning of some bits changed in port 80C, 81C, and 850.
Section 6.1.6 defines that all PCI interrupts go to 15.	PCI interrupts are routed to a single interrupt.
Section 6.3.3.1, A.1.8, and A.2.5 were changed.	System I/O bridge changed to a ZB part number.
Section 6.4 was modified to show different Endian switching and clarify that this approach applies only to 601.	Endian switching with cache enabled is easier.
Section 6.4 defines the implications on boot and Endian switching.	Endian switching is dependent upon the location of the byte reversal.
Sections 6.7.1 and 6.7.4 were changed.	Some signal names were changed.
Section 6.7.3 includes better figures and more part numbers.	To define the SRAM used in the cache.
Section A.1.2 was modified to show different Endian switching and clarify that this approach applies to other PowerPC processors.	Endian switching with cache enabled is easier.
Section A.1.2 defines the implications of boot and Endian switching.	Endian switching is dependent upon the location of the byte reversal.
Changed section A.1.13.	PCMCIA controller was changed.
Section A.4 and A.5 show more PCI adaptors.	More PCI adaptors should be included in higher-performance systems.
Clarified and expanded the implementation information in Section A.6.	Alternate interrupt structures needed for multi-processors.
Section B.4 indicates multiple apertures are an alternative.	Multiple apertures could be used to address each graphics pixel depth.

Table 1 (Page 8 of 9). History of Changes to the Specification	
Content of the Change	**Reason for the Change**
Section C.1 included.	Some devices (e.g. keyboard) are listed under a bus heading.
Expanded list of graphics adaptors in Section C.2.	Latest models of graphics adaptors were not listed.
Added PCMCIA bridges in Section C.3.	To expand the list of PCMCIA bridges.
Added explanation in Section C.5.	The 1.2 MB capacity varies the disk speed.
Section D.1 now lists the Windows NT porting center.	A Windows NT porting center is available.
Clarified processors supported in Sections D.5.1, E.5.1, and F.5.1.	Not every PowerPC processor may be supported by every operating system.
Sections D.5.5, D.12, E.5.4, E.12, F.5.4, F.5.5, and F.12 were changed to indicate what was required by the standard hardware configuration.	Some requirements for devices are not operating system requirements.
Sections D.6, E.6, and F.6 were clarified.	Tape drive is recommended as a backup medium.
Section D.8 includes a new table.	To indicate the effect on software of hardware changes.
Section E.1 contains new contact numbers.	contact numbers were incorrect.
Sections D.3, E.3, and F.3 were added.	To include some of the operating environment characteristics of the operating system.
Sections E.1 and E.4 were changed.	The AIX product plan was revamped.
Sections E.5.5 and E.5.6 were changed.	AIX is dependent upon the native attachment of devices.
Section E.8 -- removed any notion of a abstraction layer.	The AIX kernel is the software abstraction for AIX.
Reworded Section F.1.	Workplace OS is not an operating system, but a kernel which supports operating systems.
Appendix G was filled out.	Information for the Solaris operating system was obtained.
Appendix I now contains the PowerPC supplement to IEEE 1275 for Open Firmware.	To publish the PowerPC specific Open Firmware information.
The Bibliography was expanded to include every referenced document.	The Bibliography was not complete.
The Additional Information section was expanded.	To indicate where documents can be ordered.
Changes for Version 1.1	
Various clerical changes.	To correct some minor typographical errors.
Corrected references to *The PowerPC Architecture* manual in Chapter 2 and the Bibliography.	This manual is now published by an outside publisher.
Added recommendation for software in Sections 2.3.2 and 6.3.3.2.	The floppy light will light during polling.
Identified the IEEE definition of the ISA bus in Section 2.9.10.	The IEEE ISA bus document was not defined.

Table 1 (Page 9 of 9). History of Changes to the Specification	
Content of the Change	**Reason for the Change**
Clarified the resource locking information in Section 3.6.	The resource locking section needed more information.
Deleted reference in Section 3.12.1.	A doubleword byte reversal instruction was not defined.
Indicated a second source for the paper in Section 3.12.1.	To make it easier for the public to obtain technical reports.
Deleted a requirement in Section 5.1.2.	There is no reason to restrict booting to 16 colors.
Indicated in Section 5.4.1 that the boot is allowed to pass control in Little-Endian mode in some situations.	Boot should be able to pass control to Little-Endian operating systems in Little-Endian mode.
Changes made in Sections 5.5.5.1, 5.6.1 and 5.6.2.	Development has shown errors and a need for additional information in the NVRAM, Residual and PNP structures.
Defined the CRC algorithm in Section 5.5.5.2.	The CRC polynomial was not defined.
In Section 5.6, described and referenced the additional appendices.	include vendor-specific Plug and Play extensions used by AIX and a residual data dump.
Clarified in Section 6.2.5 the clock chips used in the Reference Implementation.	To define the clock chips.
In Appendix A.1.14, defined the Western Digital device.	The graphics adaptor in the Portable was not defined.
Several changes were made in Appendix A.1.	The implementation of the portable has changed slightly.
Described AIX 4.1.1 in Appendix E.	AIX has been updated since this specification was first published.
Appendix I is the updated version of the PowerPC supplement.	The PowerPC Open Firmware committee has an approved version of the supplement.
The section titled “Obtaining Additional Information” was updated.	This specification is available electronically.

1.0 Introduction

Today's computer systems exist in a wide range of environments, from hand-held portables to room-size mainframes. The largest percentage of computer systems are personal-use systems based on the IBM PC/AT*, Apple Macintosh**, or a variety of workstation-level RISC architectures. These machines cover the needs of personal productivity, entry engineering design, entry commercial data management, information analysis, and database, file, and application servers. But with all their performance and functionality, their architectures can limit the systems designer's ability to add new features without jeopardizing operating system or application compatibility. These limitations restrict the use of hardware and software enhancements which promise improved user interfaces, faster system performance, and broader operating environments.

Technological advances have outpaced the computer industry's ability to utilize them. Application and operating system compatibility issues prevent system designers from using many new architectures and interfaces. Many times, system designers must carry obsolete hardware structures to maintain compatibility. To be sustainable and continue to grow, the computer industry must define computer architectures which allow system and application designs to utilize the latest silicon, interface, storage, display and software technologies. The key to these new computer architectures is the ability of the software to abstract the hardware from the operating system kernel and applications without sacrificing compatibility or performance.

1.1 PowerPC Reference Platform Philosophy

The creators of the *PowerPC* Reference Platform Specification* believe that software, from power-on self test (POST) and diagnostics to operating systems and applications, drives the usability and acceptance of a computer system. The computer user judges the effectiveness of a system by its user environment, responsiveness, functionality, and reliability. The system software controls these attributes by leveraging the hardware features and performance to provide a total system solution.

Independent software vendors need the promise of a large installed base of hardware systems to justify the development expense for today's operating systems and applications. To create this large installed base of systems, an industry-standard computer system architecture is required. This computer system architecture must yield systems for the personal computer and workstation industry that leverage the latest digital technologies. The key features of the architecture must be: 1) its ability to allow hardware vendors to differentiate, 2) its ability to use industry-standard components and interfaces, and 3) its ability to support optimization of operating system and application performance. This type of open system architecture allows hardware system vendors to develop differentiated yet compatible systems -- each system is able to run any of the compatible operating systems as well as applications ported to those operating systems and the system architecture.

1.2 Purpose of Document

The *PowerPC Reference Platform Specification* provides a description of the devices, interfaces, and data formats required to design and build a PowerPC based industry-standard computer system. It is written to create a hardware standard, which when coupled with the hardware abstraction software provided by the operating system or hardware system vendors, allows the computer industry to build PowerPC systems which all run the same shrink-wrapped operating systems and the same shrink-wrapped applications for those operating environments. This specification defines a system architecture which covers most traditional computer systems, from portables to servers. It gives system developers the freedom to choose the level of market differentiation and enhanced features required in a given computing environment without carrying obsolete interfaces or losing compatibility.

This specification defines the minimum functional requirements needed for a compliant PowerPC Reference Platform implementation. It also provides a list of recommended hardware subsystems, devices and interfaces, which if used in a PowerPC Reference Platform implementation, yield a level of functionality required by most operating environments. This specification also describes a reference implementation which is a fully functional PowerPC Reference Platform system design supporting all operating systems and applications which are being ported to this reference platform. This Reference Implementation provides an example to which system developers can compare, allowing them a better understanding of their own design goals. The reference implementation may be built by any system vendor seeking to minimize development expense for software and hardware. But hardware platform developers maintain freedom of implementation below the level of the abstracted interfaces defined by each of the operating systems. A hardware system vendor may change subsystems from those used in the Reference Implementation. Abstraction software must be supplied for the supported operating systems by either the hardware system vendor or operating system vendor.

The *PowerPC Reference Platform Specification* is written primarily for system developers. It defines the hardware devices, subsystems, interfaces and firmware required for a compliant implementation. It contains operating system-specific descriptions and references to their hardware abstraction approach. The combination of abstraction software and this pliant hardware specification allows system vendors to differentiate while maintaining binary compatibility at the operating system and application level. This system implementation flexibility is called “compatible differentiation.” Compatibility is achieved through the use of industry-standard interfaces, system structures, device drivers, and software abstraction of hardware subsystems. The software abstraction of hardware provides expanded opportunities for differentiation by allowing enhancement of the Reference Implementation with devices abstracted from the operating systems and applications. Since abstraction layers and device drivers are operating system dependent, this differentiation comes at a cost -- differentiation requires the hardware system vendor or operating system vendor to develop software for each operating system to be supported.

Subsystem and chip vendors may also reference these specifications when developing support devices for these systems. But many of these vendors will want to consult with a system design group to understand the requirements of a given environment. It will be impossible for a single chip set to provide optimal performance and function for all cost points and all operating environments. Cost, performance, functionality, silicon process characteristics and development time will drive many design decisions.

Finally, operating system vendors may use this specification as a reference to determine the level of functionality required in a hardware abstraction layer. The specification shows the hardware subsystems which are likely to change and therefore may need hardware abstractions. Recommendations regarding the functionality of abstraction layers are also made.

1.3 PowerPC Reference Platform Goals

The goals of this specification are as follows:

- To create an open industry standard to be used for the implementation of PowerPC based systems and to support the hosting of operating systems and applications to PowerPC Reference Platforms. This specification itself is available to the industry and can be used by any hardware or software vendor to develop PowerPC products.
- To provide a specification which covers most traditional computing environments, from portables to servers. Eventually, nontraditional information systems like PDAs and Personal Communicators will be covered as addenda or new chapters to the base specification. This specification will grow as new computing environments are defined. This specification will continue to provide open industry-standard system architectures to hardware and software vendors.
- To leverage the high-volume personal computer component market for chip sets, devices and subsystems whenever possible. Many parts of a computer system need not be differentiated from other competitors.

Certain system attributes like low-speed communication ports can be easily implemented with off-the-shelf parts. Being able to use readily available personal computer components minimizes system cost; minimizes development time and expense; provides multiple suppliers; and simplifies porting of many operating systems, firmware and device drivers.

- To leverage existing and future industry-standard buses and interfaces. Existing bus architectures (i.e. ISA, VME, Micro Channel Architecture* (MCA), NuBus, etc.) provide an established base of adaptors and are well understood by card and system designers. These existing bus architectures also have a proven level of performance and functionality. Also, established industry-standard interfaces (i.e. SCSI, IDE, LocalTalk**, Ethernet**, etc.) and newer bus architectures, interfaces and protocols (i.e. PCI, PCMCIA, Serial SCSI, ATM, etc.) provide higher levels of performance or utility not achievable by the older standards. The *PowerPC Reference Platform Specification*, coupled with software abstractions of hardware and device drivers, allows the system designer to determine which buses, interfaces, and protocols best suit the target system environment.
- To allow compatible differentiation through the use of abstracted hardware interfaces and device drivers. The operating systems written for PowerPC Reference Platform-compatible systems will provide a predefined level of loadable abstractions. This allows hardware subsystem and interface variations without affecting compatibility with the operating system kernels and their respective applications. The *PowerPC Reference Platform Specification* DOES NOT define a universal BIOS in ROM because that would tie all operating systems to a single difficult-to-change interface, defined in terms of current technology. Operating systems can optimize their abstraction interfaces while supporting a wide range of environments and implementations. This structure can also leverage new software and hardware technologies without losing compatibility with older systems or applications.
- To provide address map relocation. Another key attribute of this specification is the relocatability of devices and subsystems within the PowerPC address space. Subsystem address information, which defines where I/O devices reside, is stored by the system designer and passed to the operating systems. The architecture also allows the use of multiple and identical buses and adaptors in the same system without address conflicts. This is very important in computing environments requiring a significant amount of I/O.
- To place control of power management in the operating system. It is important that the combination of hardware and software systems be designed to minimize power consumption through automatic power-saving methods. For environmental and cost reasons, systems not being used should minimize their power consumption. The goal is to have all PowerPC Reference Platform systems be power-conscious and conserve energy whenever possible.

1.4 Scope

The *PowerPC Reference Platform Specification* is targeted primarily to system design houses, but provides valuable information for operating system, device driver, adaptor, and ASIC vendors. It will also assist value-added resellers. The specification supports all 32-bit PowerPC processors. It is intended to cover the following systems: portables, medialess systems, desktops, workstations, and servers. The specification allows support for multiple operating systems, each using different methods of abstracting hardware variations. Finally, because the *PowerPC Reference Platform Specification* requires machine abstractions, the specification accommodates the evolution of software and hardware technologies without losing system compatibility.

The *PowerPC Reference Platform Specification* covers these main areas:

- Hardware Configuration

  The hardware configuration defines the minimum and recommended hardware standards and capacities required to be PowerPC Reference Platform compliant and compatible with targeted operating environ-

ments. This section describes memory system, storage media, human interfaces, I/O device and expansion requirements for a PowerPC Reference Platform-compliant system.

- Architecture

  The system architecture defines the minimum and recommended hardware system attributes required to design a compatible computer system. This section describes the key hardware and software architecture attributes and restrictions defined for PowerPC Reference Platform compliance.

- Machine Abstractions

  The Machine Abstractions section defines in general the approaches that software should take to bridge differences within PowerPC Reference Platform subsystems. Specific implementations of the machine abstraction are described and referenced in appendices for each operating system. System vendors may use this material to decide which subsystems can vary between PowerPC Reference Platform implementations.

- Boot Process and Firmware

  This section provides information on standard software features supported by ROM-based system code. This covers all code executed before control is passed to the operating system kernel. Storage locations for product configuration data are also defined. This section defines the PowerPC Reference Platform boot architecture, which supports all targeted operating systems. This section also defines the boot structure used for loading operating systems from floppy, hardfile, CD-ROM, or networks.

- Reference Implementation

  This section describes an example implementation of a PowerPC Reference Platform-compliant system. This description may be used as a high-level design for vendors wanting to produce a compatible system or may be used as an example for vendors who want to produce a differentiated system. For those who require more detail, design kits for this reference implementation are available and may be obtained through the telephone numbers listed in the section of this document entitled "Obtaining Additional Information."

1.5 PowerPC Reference Platform Brand and Certification

To support the establishment of the PowerPC Reference Platform as an open standard and to verify consistency with the architecture, a PowerPC Reference Platform brand and certification process will be established. A hardware platform which passes the hardware compliance verification may use the "PowerPC Reference Platform Compliant" brand or icon. Operating systems which pass the operating system compliance verification may also use this label. This brand will be a helpful communications tool within the marketplace, identifying systems which are ready to use compatible operating systems and applications. Also, this brand will be helpful within the development community, between system developers and operating system developers, for the communication of function and requirements.

One or more independent laboratories will be qualified to provide the *PowerPC Reference Platform Specification* certification for systems and operating systems. These laboratories will perform the verification and approve results to provide certification of a PowerPC Reference Platform-compliant hardware system or operating system.

For certification, a hardware system must demonstrate compliance to all hardware and firmware requirements in this specification in Sections 2.0, "Hardware Configuration," 3.0, "Architecture Guidance," and 5.0, "Boot Process and Firmware." The system vendor will need to provide design details to the certification laboratory in enough detail to demonstrate compliance to the requirements. The system vendor will have to provide samples of the hardware system to the certification laboratory. The certification laboratory will perform inspections and run test software on these samples.

/ In addition, a hardware system must demonstrate that it runs one of the operating systems ported to a
/ PowerPC Reference Platform. These operating systems are listed in the appendices of this specification.
/ The system vendor must provide any requisite abstraction software to the certification laboratory. The labo-
/ ratory will use a suite of functional tests to demonstrate that an operating system and some of its applica-
/ tions run on the platform. Systems certified as PowerPC Reference Platform compliant will be permitted to
/ use the brand and must identify the specific operating systems which they support. However, all operating
/ systems do not need to be certified on a vendor's system.

/ Operating systems which have been ported to PowerPC Reference Platform-compliant systems and which
/ comply with the software requirements in this document may be certified as PowerPC Reference Platform
/ compliant. Operating system requirements occur primarily in Section 4.0, "Machine Abstractions," but
/ some functions are defined in other sections. An operating system vendor would present its design and the
/ PowerPC version of the operating system to the certification laboratory. The laboratory would verify
/ through inspection and testing that the operating system met the requirements. An operating system which
/ is certified may display the PowerPC Reference Platform brand. Those that do not comply with the require-
/ ments may identify the specific hardware systems to which they have been ported.

/ Applications which have been rehosted to run on PowerPC Reference Platforms may be labeled as
/ "PowerPC Reference Platform Ready" and indicate the operating system under which the application runs.
/ No certification of applications is planned.

2.0 Hardware Configuration

/ This section describes standard subsystems that make up PowerPC Reference Platform-compliant systems.
/ The minimum compliant configuration and several other configurations are specified as sets of these subsys-
/ tems. Configuring PowerPC Reference Platform systems from standard subsystems guarantees a set of func-
/ tions and capabilities that are available to the operating systems and application software.

/ The next eight subsections discuss functions, requirements and recommendations pertaining to the processor,
/ memory, storage, human interface, Real-Time Clock, connectivity, expansion bus(es), and additional subsys-
/ tems. The ninth subsection defines interface standards for some of those subsystems. The last subsection
/ defines five typical configurations and summarizes required and recommended subsystems for each configura-
/ tion as well as for a minimum PowerPC Reference Platform-compliant machine. A table at the end of the
/ section shows the minimum requirements for a subset of each operating system targeted to be hosted on
/ PowerPC Reference Platform hardware systems.

/ Some capabilities described within this section are required to support at least one of the operating systems. These capabilities are stated in terms of "must." Every PowerPC Reference Platform-compliant machine must have these capabilities. Some capabilities are recommended for better usability or performance or to allow all operating systems to run on a PowerPC Reference Platform hardware system. These capabilities are described in terms of "recommended" or "strongly recommended." Those capabilities necessary to run all operating systems are identified. Some capabilities, while recommended in some configurations for performance reasons, are only optional in other configurations because of size, cost, power consumption or
/ other considerations. In some cases, additional information is presented to help explain the implementation
/ of these requirements and recommendations. These requirements, recommendations, and miscellaneous
/ points are intended for construction of systems in the near term. As technology evolves they will be changed so that this specification stays current.

Hardware system vendors have to build systems that run effectively across the operating environments in which they expect to market their systems. It is possible to build a PowerPC Reference Platform-compliant hardware system that supports only one of the operating systems, but this is not a recommended approach.
/ By implementing all recommended system elements and features, hardware system vendors can ensure that
/ target operating systems will be supported.

2.1 Processor Subsystem

/ This subsystem contains the processor(s) that operate on the data and instructions of the applications and
/ operating systems. Requirements, recommendations and miscellaneous information follow:

Requirements

- The processor subsystems for all compliant systems must comply fully with the PowerPC architecture.
| The PowerPC architecture is defined in *The PowerPC Architecture*, ISBN 1-55860-316-6. This architecture description is broken into three parts as defined below:

  Book I, *PowerPC User Instruction Set Architecture*
  Book II, *PowerPC Virtual Environment Architecture*
  Book III, *PowerPC Operating Environment Architecture*

- The processor subsystem time base (described in *The PowerPC Architecture*, Book III) must produce a minimum timing resolution of 500 nsec.
- The PowerPC 601 maintains a Real-Time Clock (RTC) rather than the time base. This Real-Time Clock must be driven by a 7.8125-MHz oscillator.

Recommendations

/ Processor bus frequencies of at least 20 MHz are recommended under normal operating conditions (e.g.
/ not in power savings modes).

Miscellaneous

- The architecture does not dictate the source of the time base frequency and other frequencies within the
/ system. The 603, for example, increments the time base once every four bus clocks of the local
/ PowerPC processor bus. In this case, the recommended minimum processor bus frequency of 20 MHz would support the time base resolution requirement.
/ • The PowerPC architecture requires that either a processor provide an implementation-specific interrupt
/ to software when the time base frequency is changed and provide a means to determine the current
/ update frequency, or the time base frequency must be under software control.

2.2 Memory Subsystems

Six memory subsystems are described in the following subsections: System Memory, System ROM, Non-volatile Memory, I/O Memory, System I/O, and External Cache.

2.2.1 System Memory

/ System Memory refers to the portion of the memory map for a system where executable instructions and
/ data for the applications and operating systems reside. Requirements, recommendations, and miscellaneous information follow:

Requirements

/ • A system must have a minimum of 8 MB of System Memory, but some operating systems may require
/ more.
- A system must provide for expansion of System Memory to at least 16 MB.
- System Memory must meet the coherency and serialization requirements defined in *The PowerPC Architecture*, Books II and III.
- The processors of a system must be able to read and write System Memory.
- The state of System Memory must be valid as long as power is applied to the memory subsystem.
- The System Memory must support the processor memory transactions for all target processors except as described in Section 3.17, "PowerPC Architecture Features Not Recommended." All the transactions are defined in processor-specific user's manuals.
/ • The memory controller for a system must fully decode the processor-generated addresses for System
/ Memory and must not have aliases.

Recommendations

- It is recommended that a minimum of at least 16 MB of System Memory be supplied on any system.
/ With this amount of memory, a hardware system will support any one of the operating systems that will run on PowerPC Reference Platform systems (refer to appendices).
- It is strongly recommended that a hardware system provide expansion capability of System Memory to at least 32 MB.
- It is recommended that System Memory be either parity checking or error checking and correcting (ECC).

Miscellaneous

- System Memory is normally attached to a memory controller which is located on the local primary processor bus. Expansions to System Memory are added directly to the same bus on which the base

System Memory exists. System Memory and expansions to System Memory may be located elsewhere as long as coherency is maintained. The most common implementation of main memory is DRAM.

/ • A system vendor may put I/O device memory in the System Memory area. This memory is not
/ reported as System Memory by the boot process, but is reported as part of the I/O adaptor information.
/ Operating systems will treat this memory as I/O Memory. Cache snooping is not required for addresses
/ in the range of the I/O device.

2.2.2 System ROM

/ System ROM contains the power-on and boot firmware and data required by the system. The size of System ROM is dictated by the size needed to hold the firmware required by the system. Typically System ROM is implemented using ROM, EPROM, or Flash ROM. Requirements, recommendations, and miscellaneous information follow:

Requirements

- A system must include a System ROM.
- The System ROM must be readable by the system processor.
- System ROM must maintain its state in the absence of system power.
- If System ROM is cached, then System ROM must support burst transfers to the target processor.

Recommendations

- It is strongly recommended that System ROM on all systems be writable by the system processor (e.g. Flash ROM).

Miscellaneous

- System ROM is not guaranteed to be accessible to the System I/O processors.
- 5.0, "Boot Process and Firmware," describes the functions that the firmware in System ROM may perform.

2.2.3 Non-volatile Memory

Non-volatile Memory (NVRAM) is used to save system configuration and error indications across system boots. Requirements follow:

Requirements

- A system must contain a minimum of 4 KB of Non-volatile Memory.
- Non-volatile Memory must maintain its state in the absence of system power.
- Non-volatile Memory must be readable and writeable by the system processor.

2.2.4 I/O Memory

/ I/O Memory refers to the area of the memory map of a system where memory for devices resides. This memory is accessed by a system processor using load and store instructions. Examples of I/O Memory include graphics buffers, communications buffers, and I/O processor memory. Requirements and miscellaneous information follow:

Requirements

/ • Processor-generated addresses in the I/O Memory space must be converted by the system to the
/ addresses of the I/O device on the I/O bus.
/ • The system must convert processor loads and stores for I/O Memory addresses to transfers and com-
/ mands on the I/O bus.

Miscellaneous

- I/O Memory may exist on the system expansion bus(es) and is part of the I/O subsystems. When located on these buses it is typically not cached. I/O Memory may also be located on the primary processor bus. In this case, it will participate in the hardware-managed coherency protocol, unless other ports to the same area interfere.